CHI MEI OPTOELECTRONICS CORP.

Issued Date: Jan 9, 2009
Model No.: V546H1-LH1
Approval

TFT LCD Approval Specification

MODEL NO.: V546H1- LH1

Customer: _____

Approved by: _____

Note:

Approved By	TVHD	
	LY Chen	

Reviewed By	QA Dept.	Product Development Div.
	Kc_Ko	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	WY Li	Trina Lee

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0	Nov. 12,'08	All	All	Preliminary Specification was first issued.
Ver 2.0	Jan, 01, '09	7	3.1	Updated Power Supply current spec
		9	3.2.1	Updated CCFL characteristics
		9	3.2.2	Updated Input High Voltage
		11	3.2.2	Add Backlight unit diagram
		20	6.1	Updated Input Signal Time Specifications
		20-21	6.2	Updated Internal Signal Timing Specifications
		22	6.3	Updated Power on/off sequence
		23	7.2	Updated Contrast Ratio spec
		28	9.1	Updated Packing Specifications
		28-29	9.2	Updated Packing Method
		31-32	11	Updated Mechanical Characteristic

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

V546H1-LH1 is a 54.6" TFT Liquid Crystal Display module with 22-CCFL Backlight unit and 2-ch LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 1.07G colors (10bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (500nits)
- High contrast ratio (4000:1)
- Fast response time (Gray to Gray average 4.5ms)
- High color saturation (72% NTSC)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120 Hz frame rate
- Ultra wide viewing angle: Super MVA technology

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	1209.6 (H) x 680.4 (V) (55" diagonal)	mm	(1)
Bezel Opening Area	1267.6 (H) x 738.4 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.21(H) x 0.63(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.073G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Super Clear) Hardness (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporary for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

	Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	1266.1	1267.6	1269.1	mm	(1), (2)
	Vertical (V)	737.2	738.4	739.6	mm	
	Depth (D)	38.5	40	41.5	mm	
Weight		-	19853	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	T_{ST}		-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}		0	50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	X, Y axis	-	50	G	(3), (5)
		Z axis	-	35	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}		-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

      (a) 90 %RH Max. (Ta $\leqq$ 40 ºC).

   (b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

      (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, and ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture. The module would not be twisted or bent by the fixture.

Relative Humidity (%RH)

Temperature (ºC)

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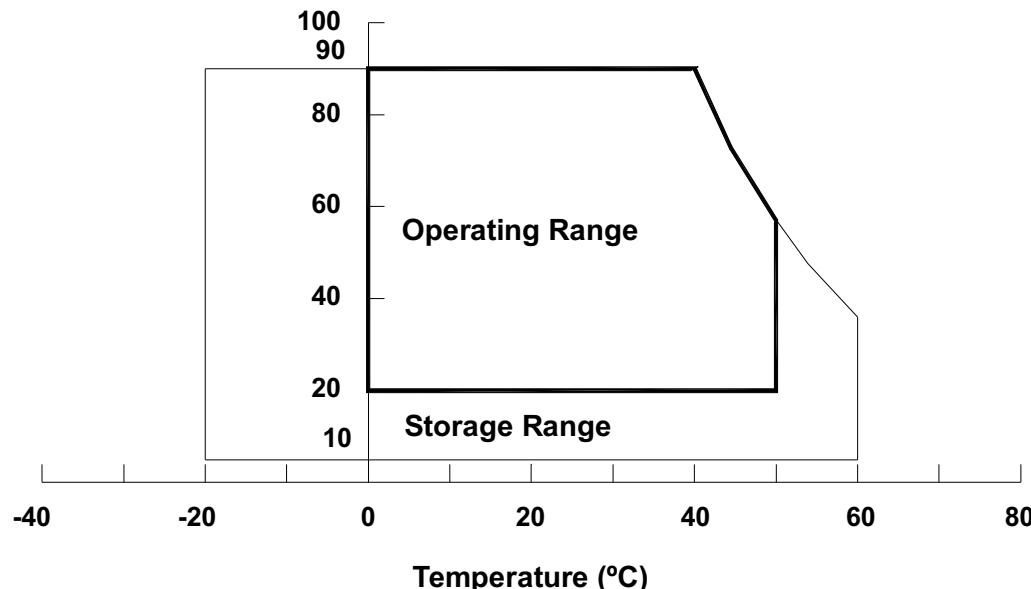
2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

2.2.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

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3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE　　(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	350	mV	
Rush Current		I_{RUSH}	-	-	6	A	(2)
Power Supply Current	White	I_{CC}	-	2.1	2.75	A	(3)
	Black		-	1.8	-	A	
	Vertical Stripe		-	2.4	2.6	A	
LVDS Interface	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T		100		ohm	
CMOS Interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:
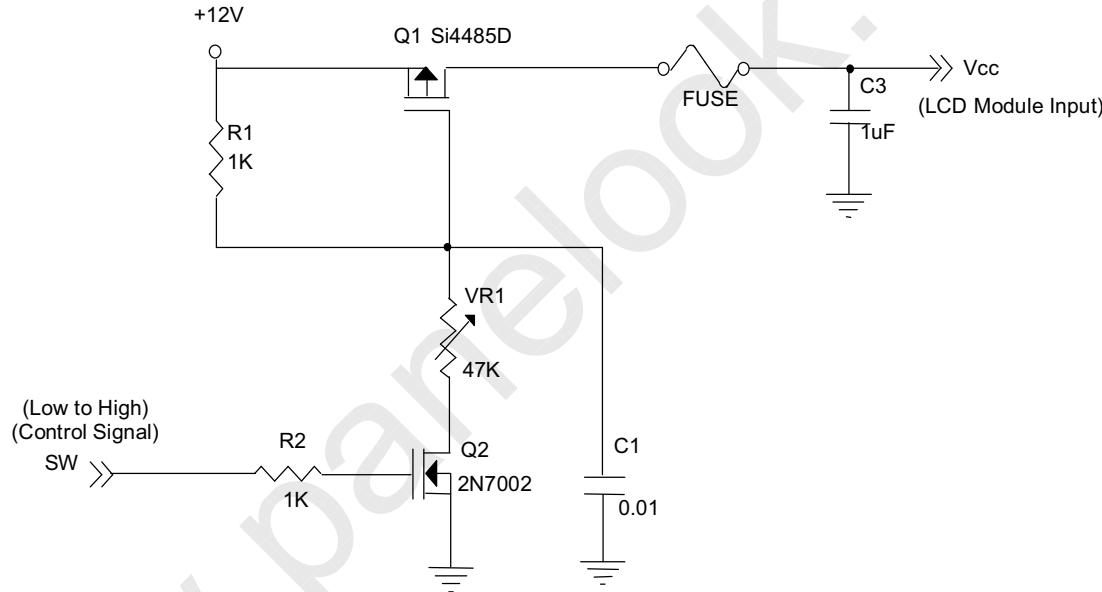
Vcc rising time is 470us
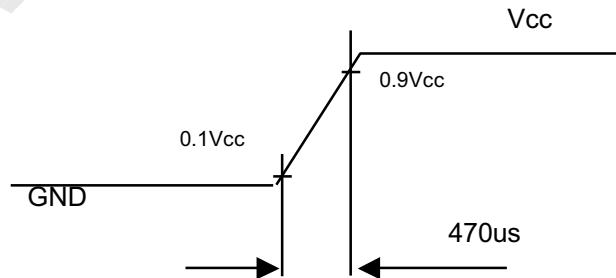
Note (3) The specified power supply current is under the conditions at Vcc = 12V, Ta = 25 ± 2 ºC, f_v = 60Hz, whereas a power dissipation check pattern below is displayed.

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a. White Pattern
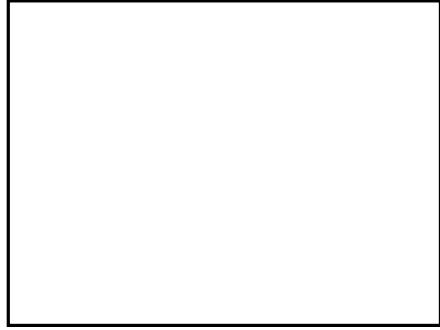
Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern

Active Area

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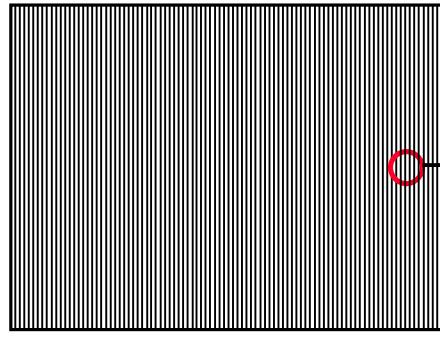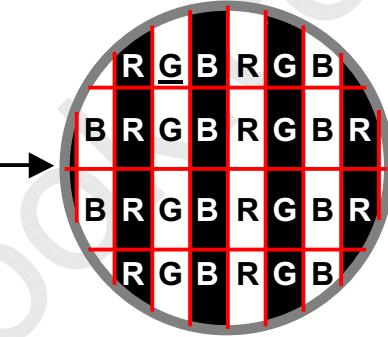
3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1440	-	V_{RMS}	-
Lamp Current	I_L	5.3	5.6	5.9	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	3165	V_{RMS}	(2), Ta = 0 ºC
		-	-	2425	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_L	35	55	80	KHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4)

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.:

Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 10.2~10.8 mArms.

3.2.2 BALANCE BOARD CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Input High Voltage		V_{HV}	-	1440	-	V	(6)
Protection Circuit Supply Voltage		Vcc	10	12	15	V	
Input Current		$I_{BL(HV)}$		125		mArms	No Dimming
Oscillating Frequency		F_W	45	48	51	kHz	
Individual Lamp Current		I_L	5.3	5.6	5.9	mA	H.V (5)
Lamp Detection	High (LD)	LD	5			V	Normal Operation
	Low (LD)	LD			1.5	V	Lamp Connector Open
Dimming frequency		F_B	135	150	165	Hz	
Minimum Duty Ratio		D_{MIN}	-	15	-	%	

Note (5) Lamp current is measured master board by utilizing high frequency current meters as shown below:

Note (6) Input voltage Hv based on spec. +-7% tolerance.

Note (7) Asymmetric ratio must be from 90% to 110% (0.9<Ip/ $I_{rms@T/2X\sqrt{2}}$ <1.1)

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Balance Board (LU)

Balance Board (LL)

LCD Module

Balance Board (RU)

Balance Board (RL)

HV (Pink +(-))
HV (White +(-))

HV -(+)

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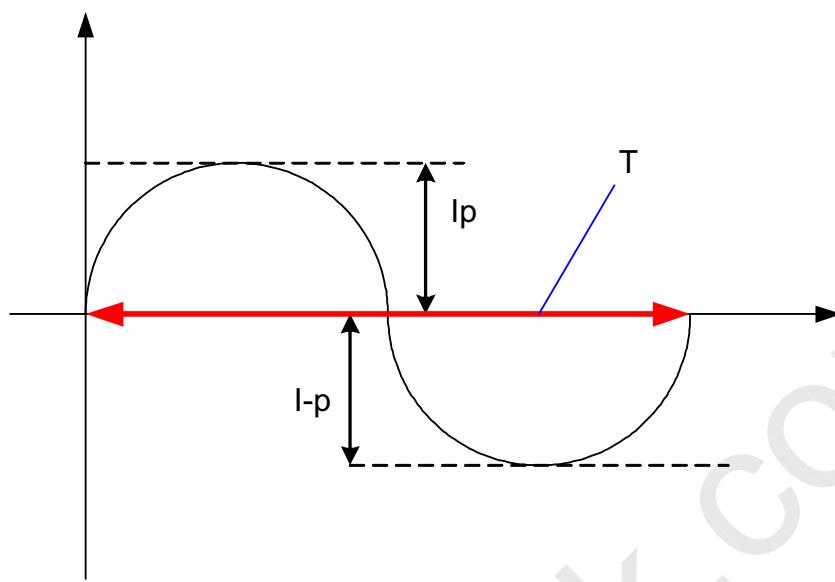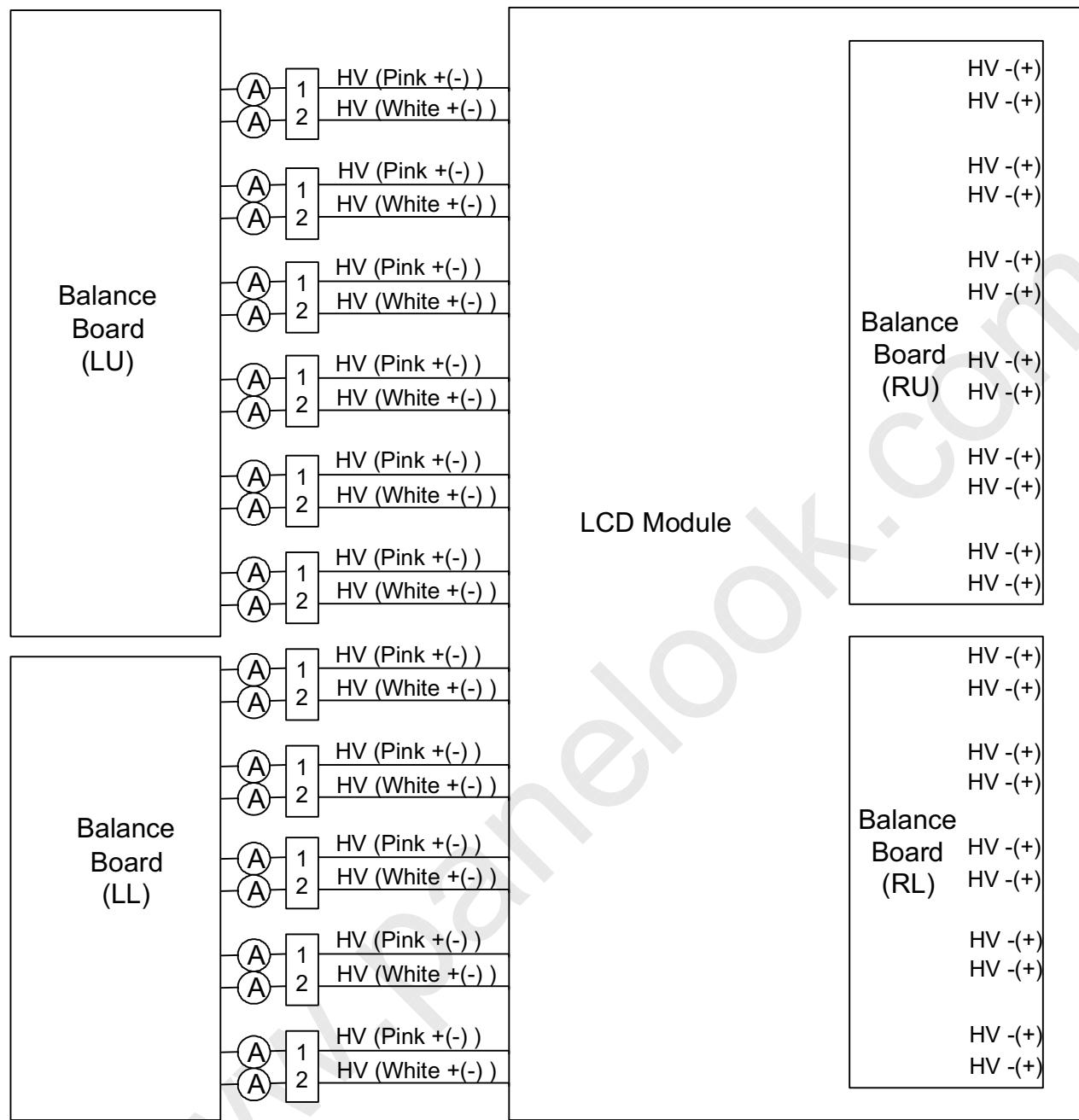
4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE

ODD_RIN0+/-
ODD_RIN1+/-
ODD_RIN2+/-
ODD_RIN3+/-
ODD_RIN4+/-
ODD_CLK+/-

EVEN_RIN0+/-
EVEN_RIN1+/-
EVEN_RIN2+/-
EVEN_RIN3+/-
EVEN_RIN4+/-
EVEN_CLK+/-

SCL_I
SDA_I
TCON_CHECK
TST_PGM
HSYNC
LVDS
I2C_SCL
FRE_NRESET
I2C_SDA
SW_PVCC
MAIN_CHECK

VIN
GND

INPUT CONNECTOR (FI-RE51S-HF (JAE))

FRAME BUFFER

TIMING CONTROLLER

DC/DC CONVERTER & REFERENCE VOLTAGE GENERATOR

SCAN DRIVER

TFT LCD PANEL (1920x3x1080)

DATA DRIVER (RSDS)

CN3-CN13 (Master): SM02-BDAS-3-TB (JST)

BALANCE BOARD CONNECTOR

CN1 (LL): SM02-BDAS-3-TB (JST)

BACKLIGHT UNIT

BALANCE BOARD CONNECTOR

CN1 (RL): SM02-BDAS-3-TB (JST)

+(-) HV   **IP board**   -(+) HV

CN33: KN30-7P-1.25H (Hirose)

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5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module

Pin	Name	Description
1	VIN	+12.0V power supply
2	VIN	+12.0V power supply
3	VIN	+12.0V power supply
4	VIN	+12.0V power supply
5	VIN	+12.0V power supply
6	NC	No connection
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	ODD_RIN0N	Negative transmission data of First pixel 0
11	ODD_RIN0P	Positive transmission data of First pixel 0
12	ODD_RIN1N	Negative transmission data of First pixel 1
13	ODD_RIN1P	Positive transmission data of First pixel 1
14	ODD_RIN2N	Negative transmission data of First pixel 2
15	ODD_RIN2P	Positive transmission data of First pixel 2
16	GND	Ground
17	ODD_RINCLKN	Negative of First clock
18	ODD_RINCLKP	Positive of First clock
19	GND	Ground
20	ODD_RIN3N	Negative transmission data of First pixel 3
21	ODD_RIN3P	Positive transmission data of First pixel 3
22	ODD_RIN4N	Negative transmission data of First pixel 4
23	ODD_RIN4P	Positive transmission data of First pixel 4
24	GND	Ground
25	EVEN_RIN0N	Negative transmission data of Second pixel 0
26	EVEN _RIN0P	Positive transmission data of Second pixel 0
27	EVEN _RIN1N	Negative transmission data of Second pixel 1
28	EVEN _RIN1P	Positive transmission data of Second pixel 1
29	EVEN _RIN2N	Negative transmission data of Second pixel 2
30	EVEN _RIN2P	Positive transmission data of Second pixel 2
31	GND	Ground
32	EVEN _RINCLKN	Negative of Second clock
33	EVEN _RINCLKP	Positive of Second clock
34	GND	Ground
35	EVEN _RIN3N	Negative transmission data of Second pixel 3
36	EVEN _RIN3P	Positive transmission data of Second pixel 3
37	EVEN _RIN4N	Negative transmission data of Second pixel 4
38	EVEN _RIN4P	Positive transmission data of Second pixel 4
39	GND	Ground
40	SCL_I	SEC define

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41	SDA_I	SEC define
42	TCON_CHECK	SEC define
43	TST_PGM	SEC define
44	HSYNC	SEC define
45	LVDS_FORMAT	SEC define
46	I2C_SCL	SEC define
47	FRC_NRESET	SEC define
48	I2C_SDA	SEC define
49	SW_PVCC	SEC define
50	MAIN_CHECK	SEC define
51	NC	No connection

Note (1) CN505 Connector Part No.: JAE Taiwan(台灣航空電子) FI-RE51S-HF or equal.

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5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN3-CN13: SM02-BDAS-3-TB (JST)

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model SM02-BDAS-3-TB,

　　　　manufactured by JST. The mating header on inverter part number is

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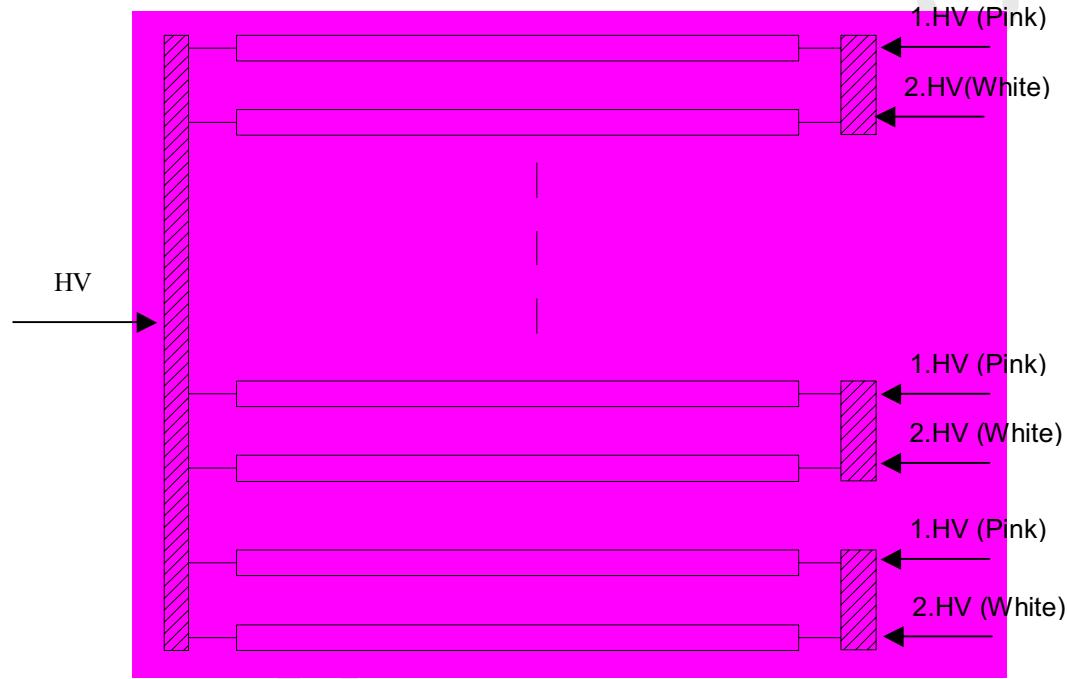
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5.3 BALANCE BOARD UNIT

CN1 (Header) (RU & RL): SM02-BDAS-3-TB (JST)

Pin No.	Symbol	Description
1	HV+(-)	High Voltage Input
2	HV+(-)	High Voltage Input

CN2 (Header) (Master): SM02-BDAS-3-TB (JST)

Pin No.	Symbol	Description
1	HV-(+)	High Voltage Input
2	HV-(+)	High Voltage Input

CN3-CN13 (Header) (RU & RL): SM02-BDAS-3-TB (JST)

Pin No.	Symbol	Description
1	CCFL HOT	CCFL High voltage
2	CCFL HOT	CCFL High voltage

CN33 (Header): KN30-7P-1.25H (Hirose).

Pin No.	Symbol	Description
1	VCC	Power Supply for Protection Circuit
2	FB1	Lamp Current Feedback 1
3	FB2	Lamp Current Feedback 2
4	GND	Signal Ground
5	GND	Signal Ground
6	LD	CCFL Connector Open & Non-lighting signal
7	LD	CCFL Connector Open & Non-lighting signal

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5.4 BLOCK DIAGRAM OF INTERFACE

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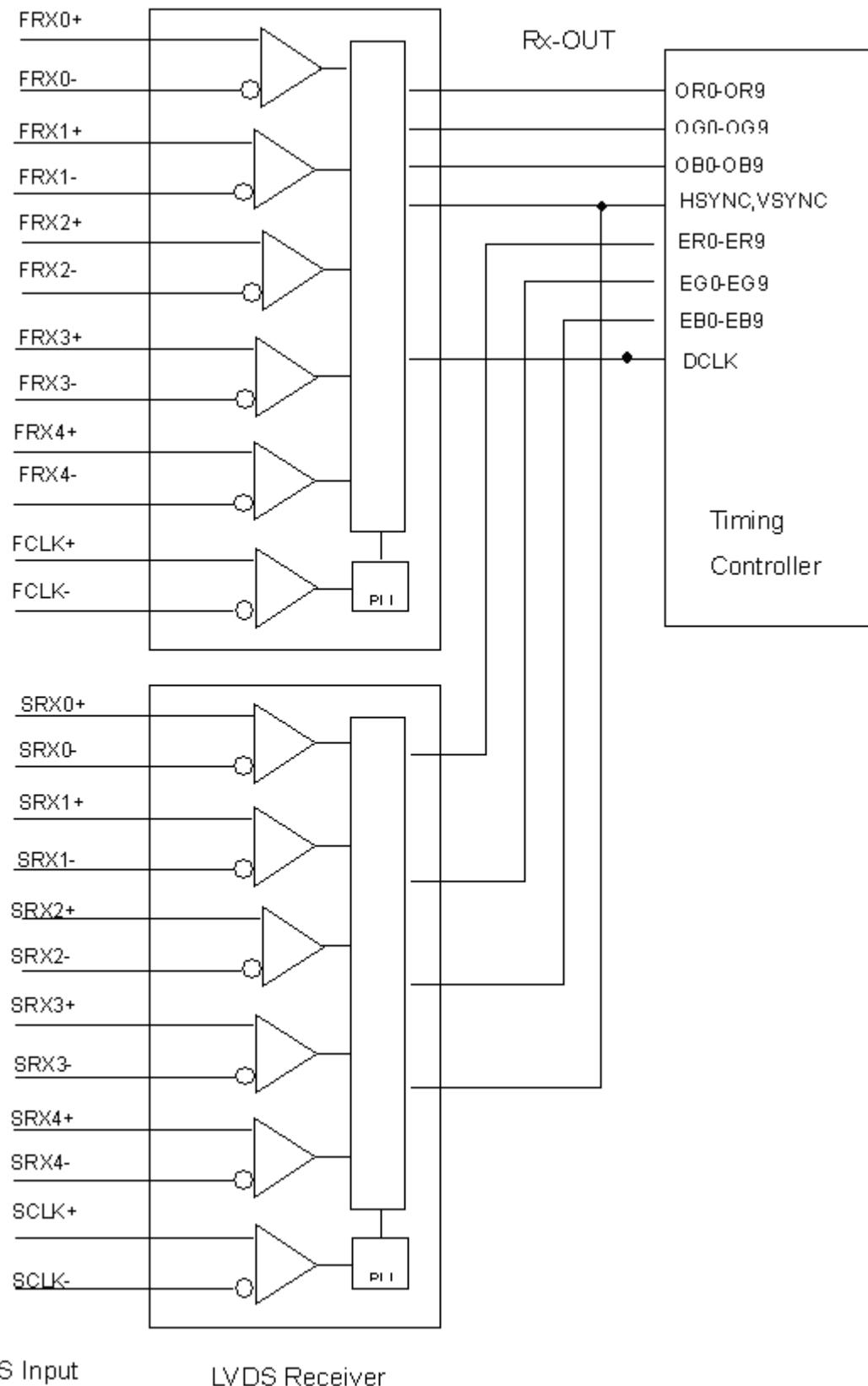
5.5 LVDS INTERFACE

VESA Format : SELLVDS = H or Open

JEIDA Format : SELLVDS = L
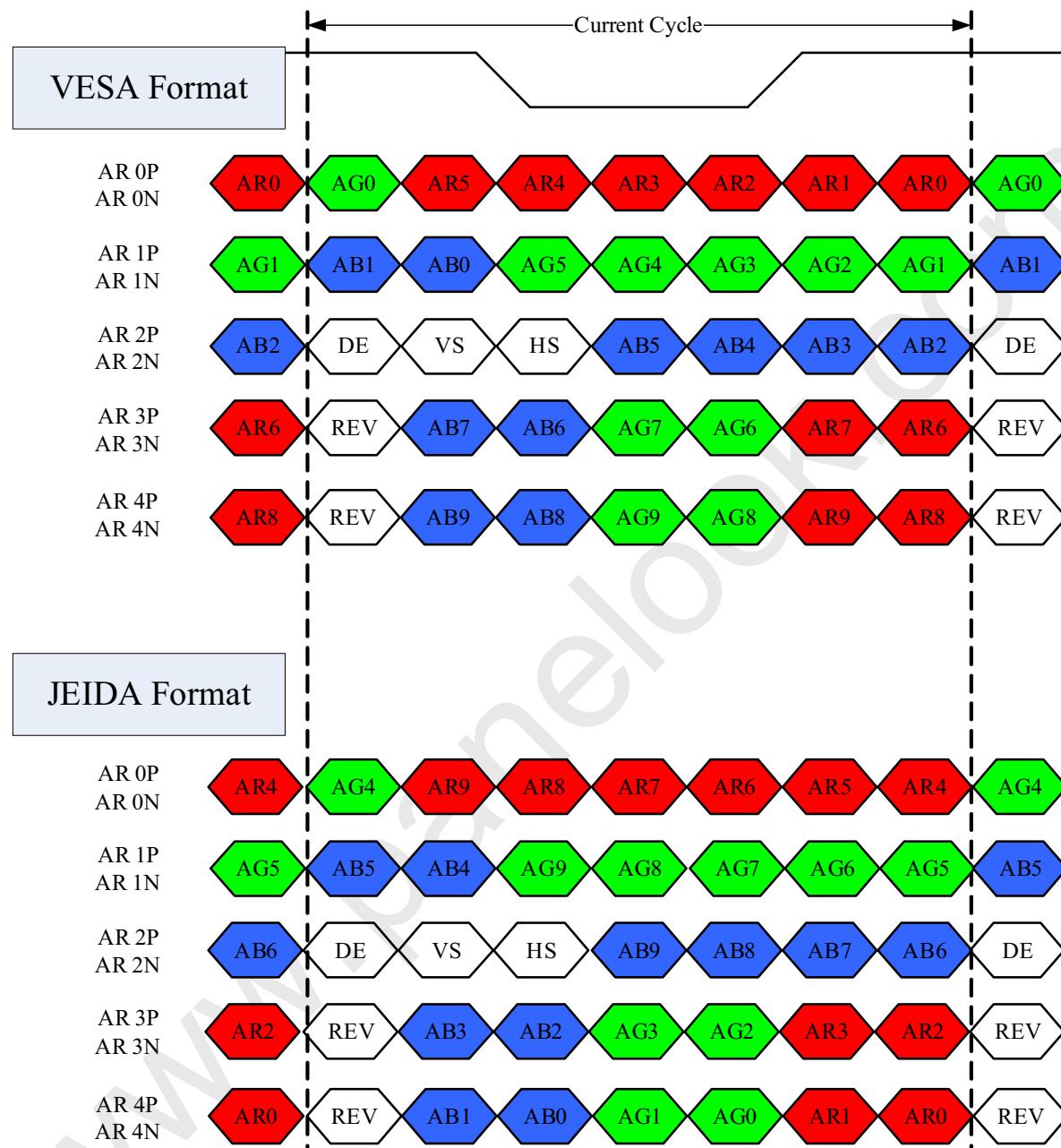
AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE   : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

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5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																														
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
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	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	-	74	-	MHz	-
Hsync		F_H	-	67.5	-	KHz	-
Vsync		F_V	-	59.94	-	Hz	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr6	57	60	63	Hz	
	Total	Tv	-	1125	-	Th	Tv=Tvd+Tvb
	Display	Tvd	-	1080	-	Th	-
	Blank	Tvb	-	45	-	Th	-
Horizontal Active Display Term	Total	Th	-	2200	-	Tc	Th=Thd+Thb
	Display	Thd	-	1920	-	Tc	-
	Blank	Thb	-	280	-	Tc	-

. 6.2 INTERNAL SIGNAL TIMING SPECIFICATIONS (FRC→ T-CON)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74	80	MHz	(1)
Hsync		Fh	-	135	-	KHz	
Vsync		Fv	-	120	-	Hz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr6	-	120	-	Hz	
	Total	Tv	1115	1125	1139	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	59	Th	-
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	-
	Blank	Thb	60	70	95	Tc	-

Note : Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note(1) : LVDS Clock should not over 80MHz even if H-total or V-total is in spec, and the frequency follows the equation below.

LVDS CLK= Frame rate * H-total * V-total

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INPUT SIGNAL TIMING DIAGRAM

T_v

T_{vd}

T_{vb}

DE

T_h

DCLK

T_c

DE

T_{hb}

T_{hd}

DATA

Valid display data (960 clocks)
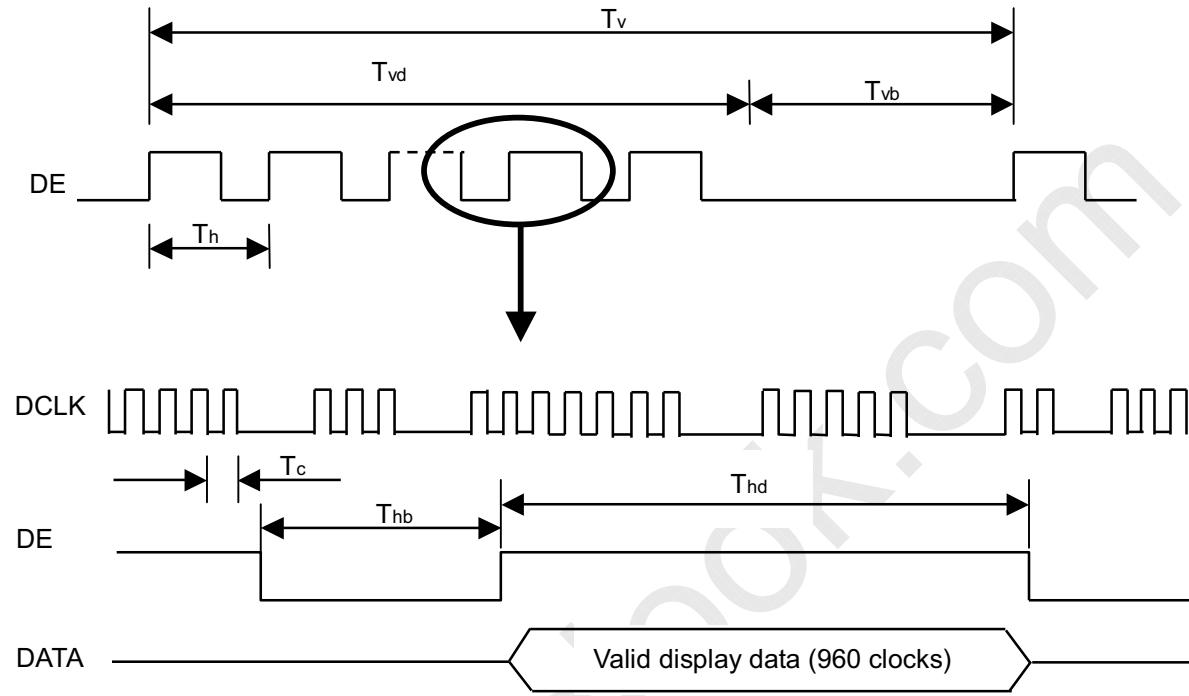
LVDS RECEIVER INTERFACE TIMING DIAGRAM

Tc

RXCLK+/-

RXn+/-

Tlvsu

Tlvhd

$\dfrac{1T}{14}$ $\dfrac{3T}{14}$ $\dfrac{5T}{14}$ $\dfrac{7T}{14}$ $\dfrac{9T}{14}$ $\dfrac{11T}{14}$ $\dfrac{13T}{14}$

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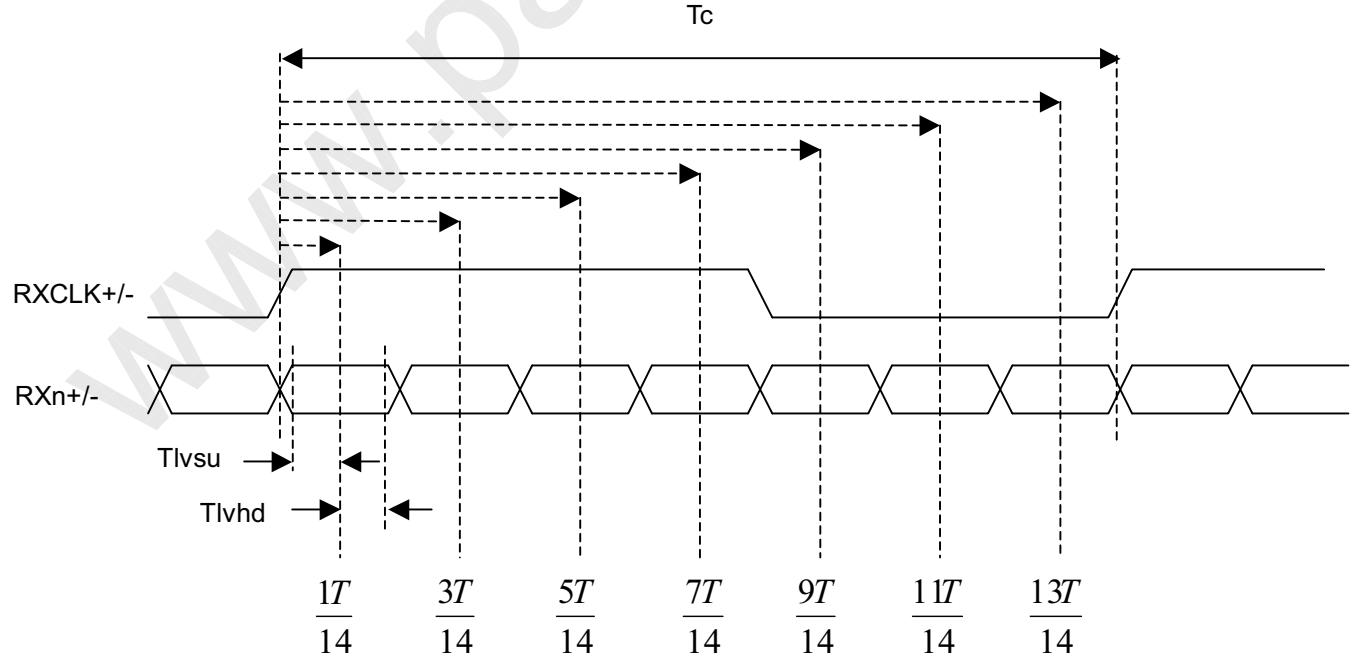
6.3 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.

$0 \leqq T_1 \leqq 10$ ms
$0 \leqq T_2 \leqq 50$ ms
$0 \leqq T_3 \leqq 50$ ms
1000 ms $\leqq T_4$

$0 \leqq T_7 \leqq T_2$
$0 \leqq T_8$

Option Signals
(SELLVDS)

Backlight (Recommended)
1000 ms$\leqq T_5$
100 ms$\leqq T_6$

VALID

Power On   Power Off

Power ON/OFF Sequence
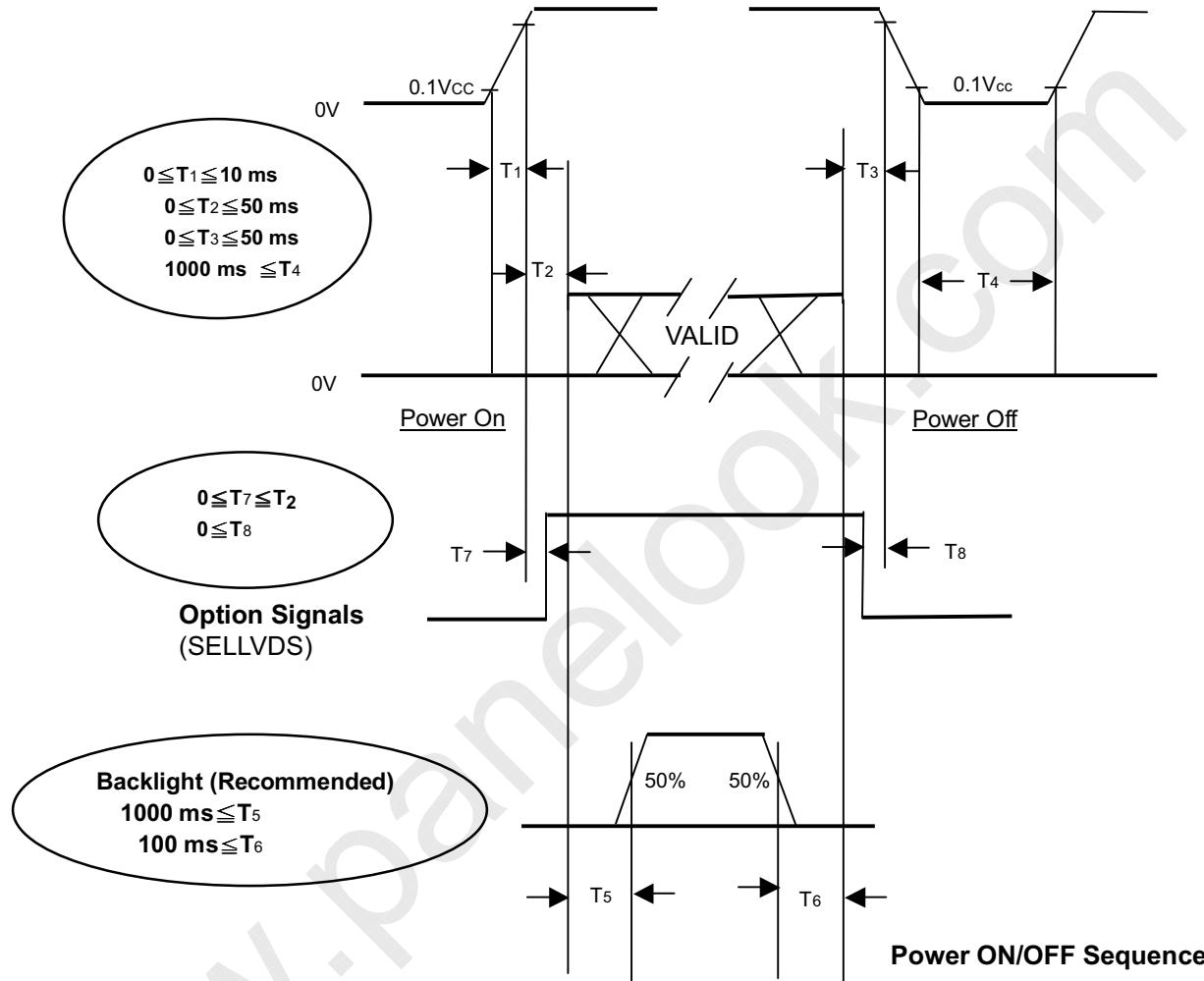
Note：

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

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7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	^oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	5.6±0.3	mA
Oscillating Frequency (Inverter)	F_W	48±3	KHz
Vertical Frame Rate	Fr	120	Hz

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		(3000)	(4000)	-	-	Note (2)
Response Time		Gray to gray		-	(4.5)	12	ms	Note (3)
Center Luminance of White		L_C		450	500	-	cd/m^2	Note (4)
White Variation		δW		-	-	1.3	-	Note (7)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx	$\theta_x=0°$, $\theta_Y=0°$ Viewing angle at normal direction	Typ.-0.03	0.643	Typ.+0.03	-	Note (6)
		Ry			0.326		-	
	Green	Gx			0.293		-	
		Gy			0.599		-	
	Blue	Bx			0.150		-	
		By			0.061		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Color Gamut				72	-	%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	Note (1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

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Note (1) Definition of Viewing Angle (θx, θy):

     Viewing angles are measured by Eldim EZ-Contrast 160R

Normal

θx = θy = 0°

θy- θy+

θx- = 90°   x-

12 o'clock direction

θy+ = 90°

θx−   y+

θx+

6 o'clock

θy- = 90°   y-

x+ θx+ = 90°
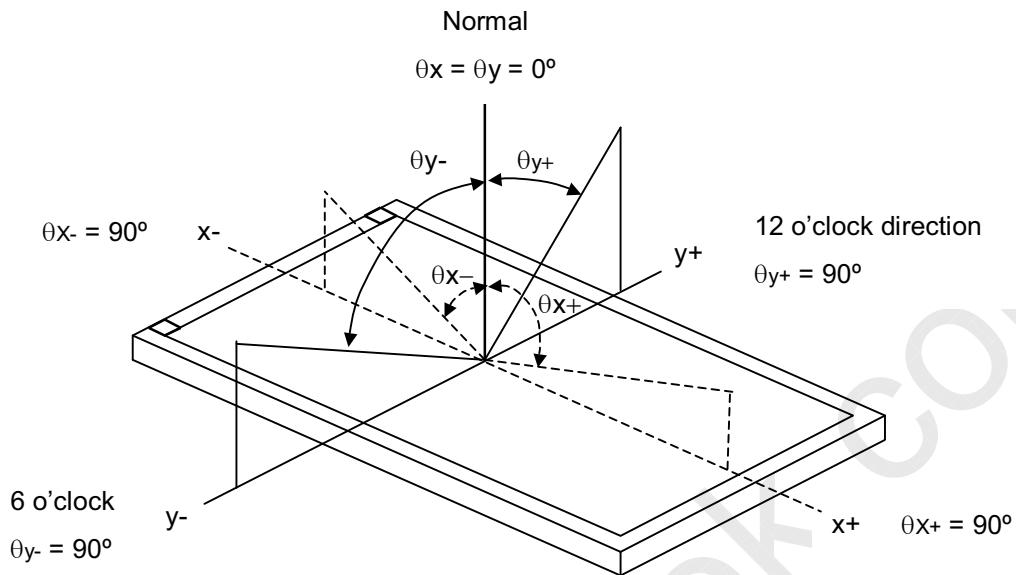
Note (2) Definition of Contrast Ratio (CR):

     The contrast ratio can be calculated by the following expression.

       Contrast Ratio (CR) = L255 / L0

       L255: Luminance of gray level 255

       L 0: Luminance of gray level 0

       CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note

       (7)

Note (3) Definition of Gray to Gray Switching Time :

100%
90%

Optical

Response

10%
0%

Time

Gray to gray
switching time

Gray to gray
switching time
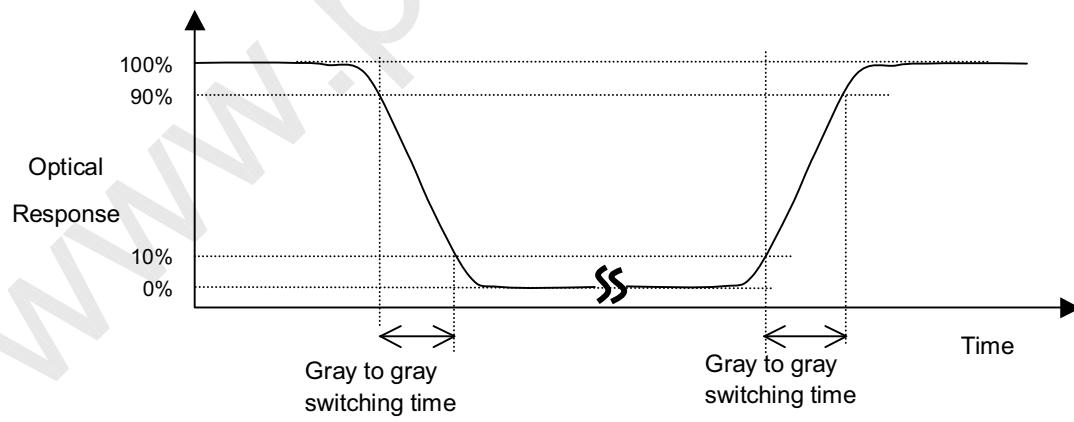
  The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

  Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each

  other .

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Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point.

L_C = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

Note (5) Definition of Cross Talk (CT):

CT = | $Y_B - Y_A$ | / $Y_A \times$ 100 (%)

Where:

(a)

Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)
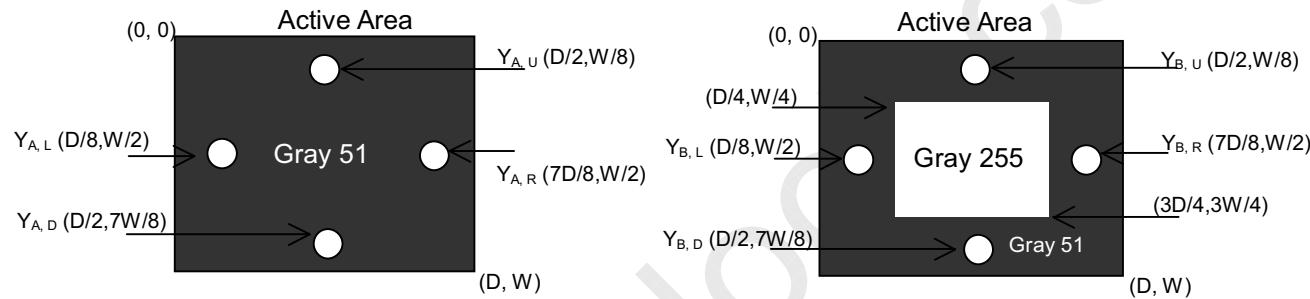
(b)

Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)


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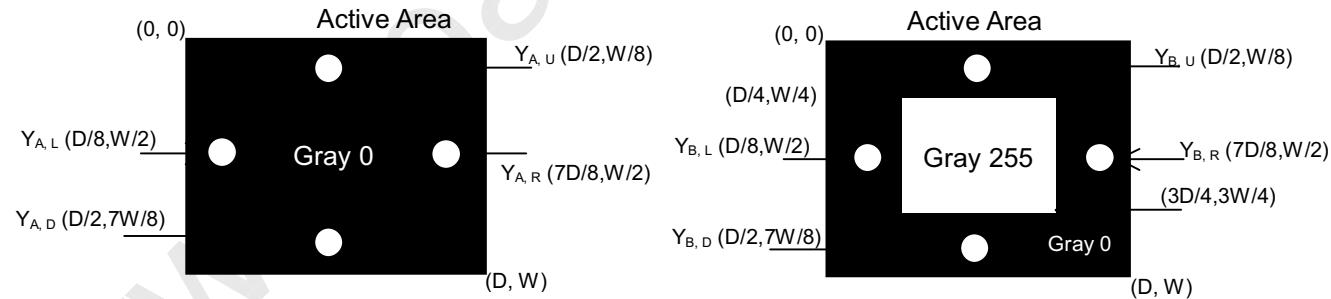
Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.
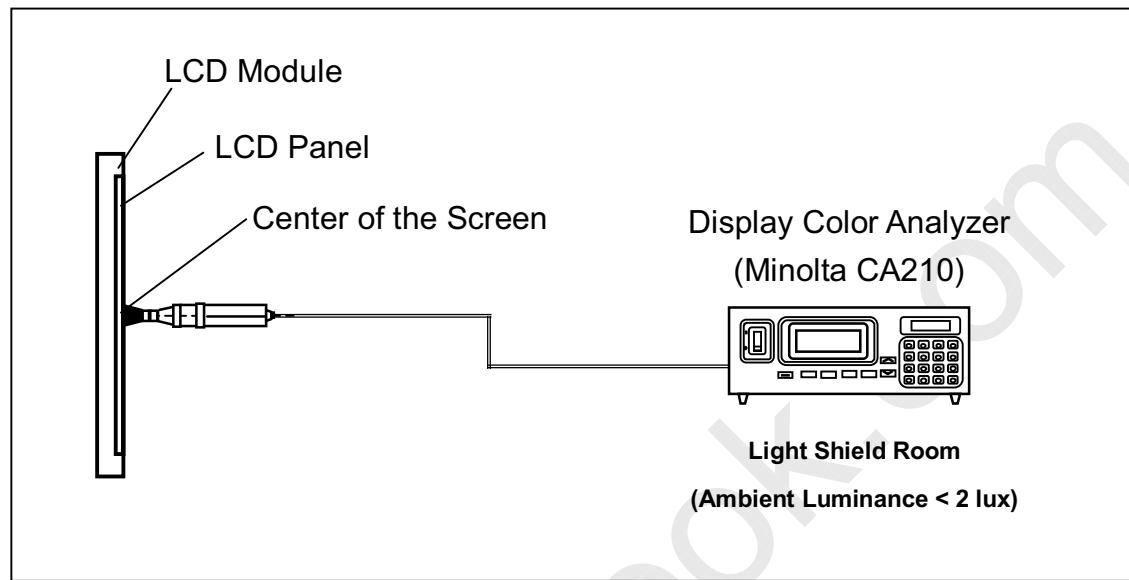
Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

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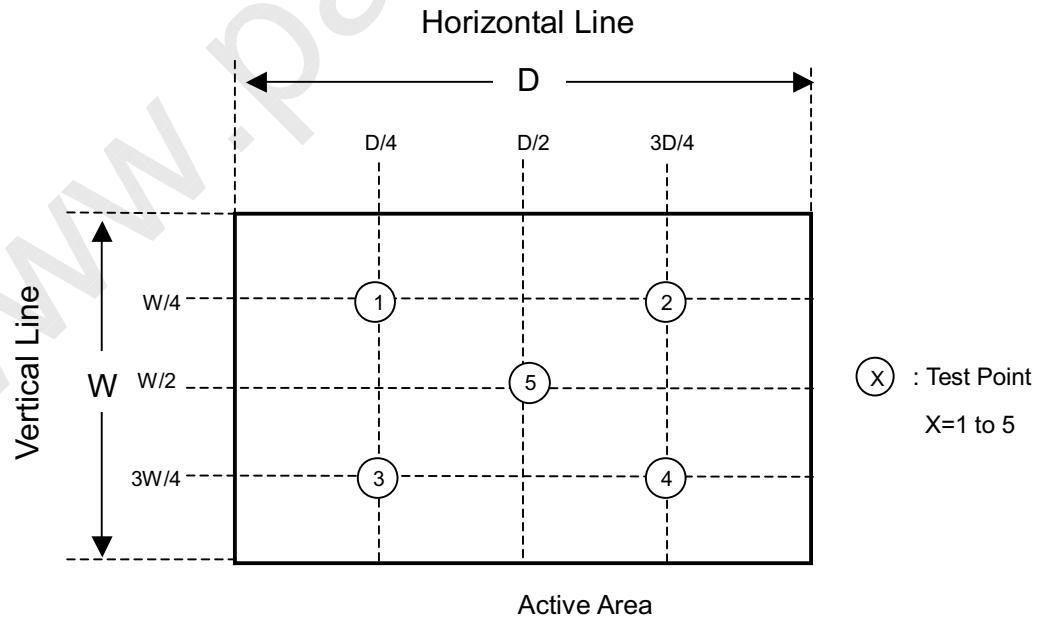
8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

```
CHI  MEI              V546H1        -LH1 Rev. XX                 cULus ®
OPTOELECTRONICS      |||||||||||||||||||||||||||||||||||         E207943
                      X X X X X X X Y M D L N N N N              MADE IN TAIWAN

                     |||||||||||||||||||||||||||||||||||||||||||
                           CM54H11XXXXXLXXLYMDNNNN
```
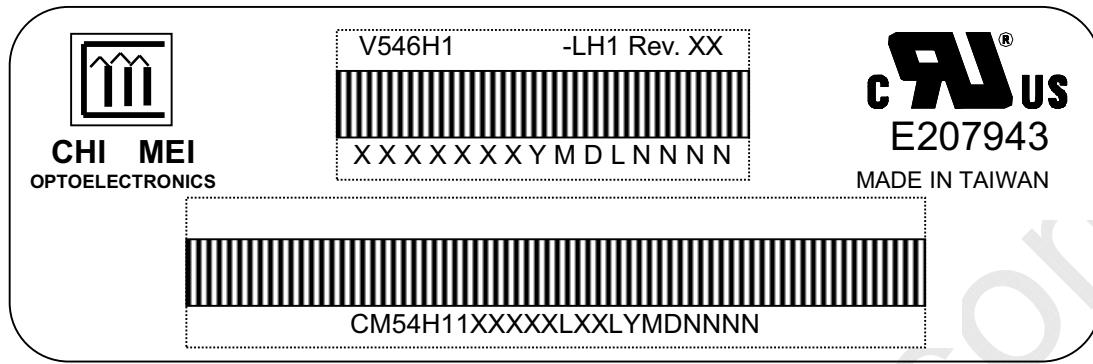
(a) Model Name: V546H1-LH1

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X-XX	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4… Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1st to 31st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
L	Product line #	Line 1=1, Line 2=2, Line 3=3, …
NNNN	Serial number	Manufacturing sequence of product

(d) Customer's barcode definition:

Serial ID: CM-46H15-X-X-X-XX-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMO=CM
46H15	Model number	V546H1-LH1=54H11
X	Revision code	C1=A, C2=B,…
X	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatec=C,
X	Gate driver IC code	OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	1~12=0~C
XX	Module location	Tainan, Taiwan=TN
L	Module line #	1~12=0~C
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4… Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1st to 31st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
NNNN	Serial number	By LCD supplier

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9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 2 LCD TV modules / 1 Box

(2) Box dimensions: 1334(L) X 284 (W) X 856 (H)

(3) Weight: approximately 46 Kg (2 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method
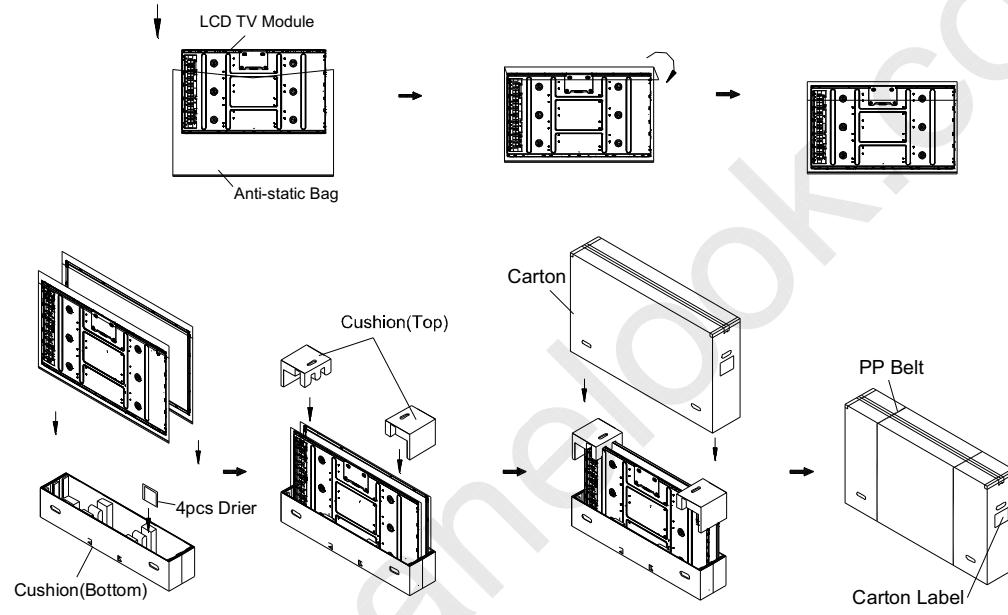

Figure.9-1 packing method

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Sea & Land Transportation
Gross : 383Kg
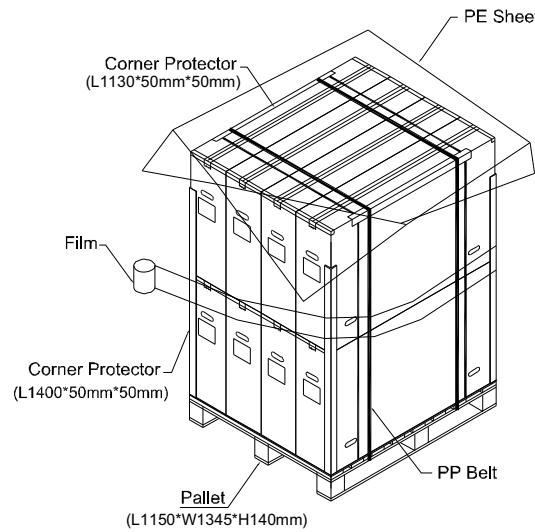
Air Transportation
Gross : 199Kg

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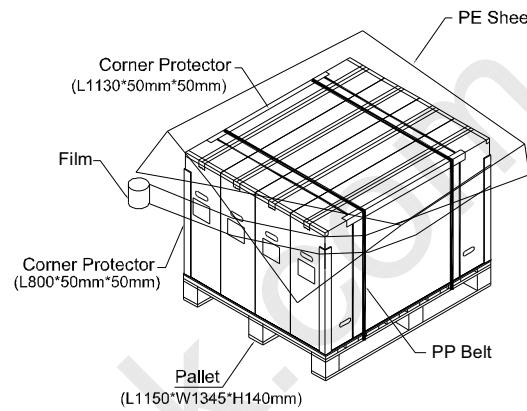
10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

10.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL 60950-1: 2003
	cUL	CAN/CSA C22.2 No.60950-1-03
	CB	IEC 60950-1:2001
Audio/Video Apparatus	UL	UL 60065: 2003
	cUL	CAN/CSA C22.2 No.60065-03
	CB	IEC 60065:2001

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

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11. MECHANICAL CHARACTERIST

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